cont. B1

an output portion 72. The output portion 72 includes a mixer 74 that receives the analog signal on signal line 70 and feeds a transmitter 76, which in turn transmits the signal. DAC can be used in any digital to analog conversion.

Please replace the paragraph beginning on line 21, page 20, with the following:

FIG. 15 is a block diagram of another embodiment of the SC DAC 150, which is similar to the SC DAC 150 illustrated in FIGS. 13, 14A-14C, except that the SC DAC 150 of FIG. 15 further comprises a switch S48, a switch S49, and a switch S50. A first terminal of the switch S48 is connected to the second terminal of the charge sharing switch S43. A first terminal of the switch S49 is connected to the second terminal of the charge sharing switch S45. A first terminal of the switch S50 is connected to the second terminal of the charge sharing switch S46. Each of the switches S48, S49, and S50 may, but need not serve one or more of the functions noted hereinbelow. In one embodiment, one purpose of the switches S48, S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47.

B2

In the Claims

Please amend the claims as follows:

B3

5. (Amended) The DAC of claim 1, wherein for each of the plurality of sub DACs, the associated capacitance comprises a single capacitor.

B4

13. (Amended) The DAC of claim 12, wherein for each of the plurality of sub DACs, the associated capacitance comprises a single capacitor.

37. (Twice Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the integrated switched capacitor network having a charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another, and

B5